DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 5/8/08 has been considered by the examiner.

Response to Amendment

Examiner notes Applicant has appointed a new power of attorney as of 2/4/08.

Examiner further notes the correspondence on 6/13/08, from the original attorney of record, was improper and should not have been entered since the correspondence was not from the attorney of record.

This office action is in response to the amendment filed 5/8/08. Accordingly, the finality of the last Office action, sent 7/14/08 is withdrawn to respond to the appropriate claims filed 5/8/08. This office action replaces the prior office action sent 7/14/08.

The period for reply has been reset and a new shortened statutory period shall take effect from the mailing date of this action.

Response to Arguments

Applicant's arguments with respect to the amended claims filed 5/8/08 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

The drawing of Figure 2 was received on 5/8/08. The drawing is not acceptable because it is unclear what the dashed line represents and what boxes 26 and 27 represent.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the output terminal connected between the amplifying element and the current sensor, as in Claim 6, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 9 is objected to because of the following informalities: 'the source' and 'the transistor' lack antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dening (US 6,329,809) in view of Hardee (US 5,570,005).

With respect to Claim 2, Dening discloses a capacitive feedback circuit (Fig. 4 C1a,R1a,412,R2a,BIAS) comprising:

a voltage input terminal (Fig. 4 402); a current output terminal (Fig. 4 node R2a,C2a);

a feedback capacitor (Fig. 4 C1a), having a first terminal connected to input terminal (Fig. 4 402) and having a second terminal connected to a high-impedance [R1a is orders of magnitude larger than R1] node (Fig. 4 node C1a-412);

a current amplifying element (Fig. 4 412) having a high-impedance control terminal connected to said node;

a current sensor (Fig. 4 R2a) connected in series between said current amplify element (Fig. 4 412) and a first supply voltage (Fig. 4 BIAS). Dening does not detail the bias generator.

Hardee teaches a bias generator (Fig. 1 10) with a first supply voltage (Fig. 1 VCC), a bias current source (Fig. 1 24 sources current) connected in series between a load (Fig. 1 30) and a second supply voltage (Fig. 1 VCCEXT). It would have been

obvious to one of ordinary skill in the art at the time of the invention to connect VCC as the first supply voltage [voltage BIAS to resistor R2a]. The reason for doing so is "to receive the input supply voltage and generate a controlled low voltage signal. Because the low voltage signal is controlled, this signal can be used within the circuit to drive circuits or generate other signals which are independent of variations in the input supply voltage" (Hardee column 1, lines 63-67).

With respect to Claim 5, Dening in view of Hardee the capacitive feedback circuit according to claim 2, wherein the output terminal is connected to a node (Fig. 4 C2a-R2a) between the current amplifying element (Fig. 4 412) and the bias current source (Fig. 4 BIAS).

With respect to Claim 6, Dening in view of Hardee disclose the capacitive feedback circuit according to claim 2, wherein the output terminal is connected to a node (Fig. 4 C2a-R2a) between the current amplifying element (Fig. 4 412) and the current sensor (Fig. 4 R2a).

Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dening (US 6,329,809) in view of Hardee (US 5,570,005) and further in view of Cali (US 6,265,856).

With respect to Claim 8, Dening in view of Hardee disclose the capacitive feedback circuit as set forth above and do not detail the structure of the step down

converter. Cali teaches a step down converter (Fig. 3) having a second transistor (Fig. 3 M2) connected to a second supply voltage (Fig. 3 Vpos) with a gate connected to a constant bias voltage (Fig. 3 Vg2). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the step down converter as a linear regulator with breakdown protection. The reason for doing so is “to prevent breakdown of the output PMOS transistor when the regulator is in the "off" state” (Cali column 2, lines 45-48).

With respect to Claim 9, Dening in view of Hardee and Cali disclose the circuit as set forth above wherein the second transistor (Fig. 3 M2) has its drain connected to a source of a first transistor (Fig. 3 M1).

Claims 10 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dening (US 6,329,809) in view of Hardee (US 5,570,005) and further in view of Wrathal (US 5,867,014).

With respect to Claim 10, Dening in view of Hardee disclose a circuit as set forth above wherein the current sensor is a sense resistor, and do not disclose using a current mirror configuration to sense the current. Wrathal teaches using a current mirror configuration to sense the current. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a current mirror configuration to sense the current. The reason for doing so is to prevent the power loss of the sense resistor.

With respect to Claim 16, Dening in view of Hardee disclose a circuit as set forth above and do not disclose regulating the supply voltage (Dening Fig. 4 VCC) based upon the load current (Dening Fig. 2 Iout). Wrathal teaches a voltage regulator sensing the load current. It would have been obvious to one of ordinary skill in the art at the time of the invention to regulate the supply voltage VCC to the power circuit (Fig. 4 400) based upon the sensed load current (Fig. 4 PWR SENSE). The reason for doing so is "There are numerous applications in which current through a circuit load is to be regulated. Current regulation is used to protect circuitry from being damaged in a short circuit or overload situation. For example, the current through a power transistor of a power supply may be monitored to provide a means for limiting current flow through circuitry powered by the supply" (Wrathal column 1, lines 11-17).

Allowable Subject Matter

Claim 17 is allowed. See the action dated 12/14/07 for reasons for allowance.

Claims 3-4, 7 and 11-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: With respect to Claim 3, the prior art does not disclose or suggest, in combination with the limitations of the base claim and any intervening claims, primarily, wherein said current sensor is part of a current-to-voltage converting feedback loop, which has a high-impedance output terminal connected to said node.

The aforementioned limitations in combination with all remaining limitations of the respective claims are believed to render the aforementioned indicated claim and any dependent claims thereof patentable over the art of record.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HARRY BEHM whose telephone number is (571)272-8929. The examiner can normally be reached on 7:00 am - 3:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm E. Ullah can be reached on (571) 272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Harry Behm/
Examiner, Art Unit 2838

/Jeffrey L. Sterrett/
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